AIC Final Project 105061129楊詠旭

1. Schematic

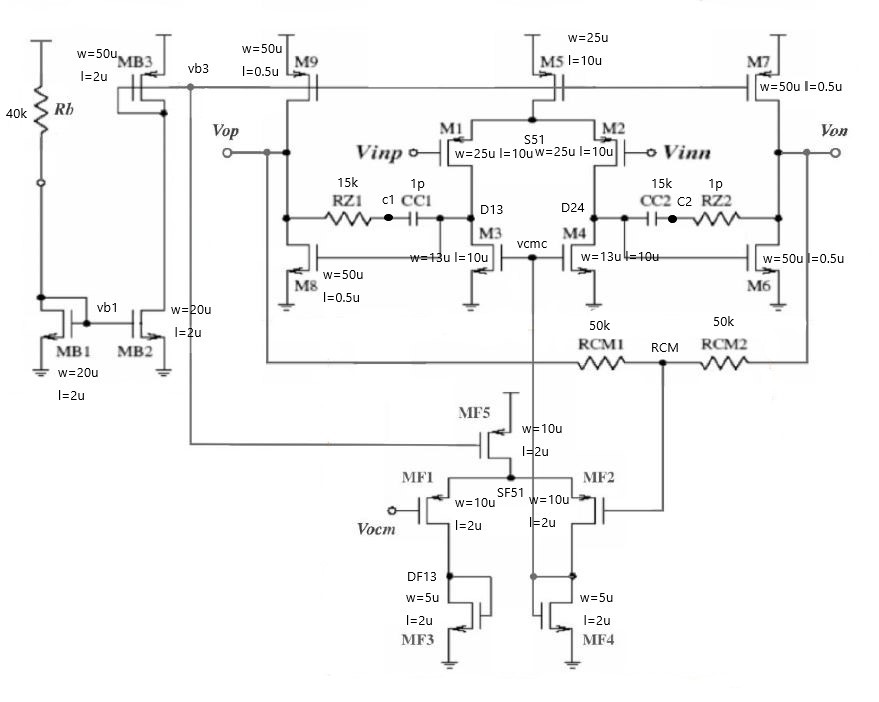


Fig. 1(a) active device size & passive component value

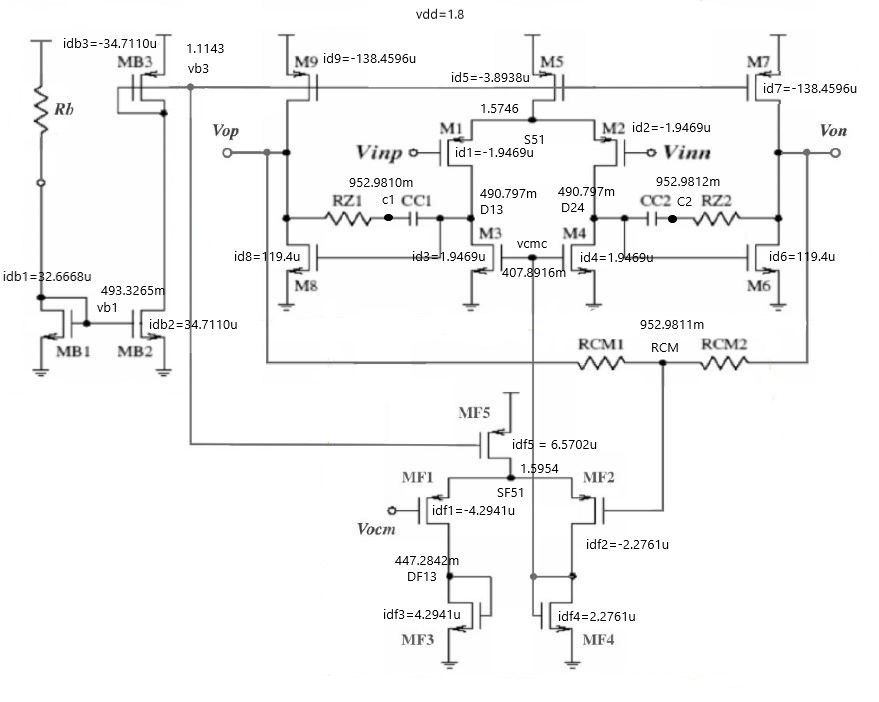
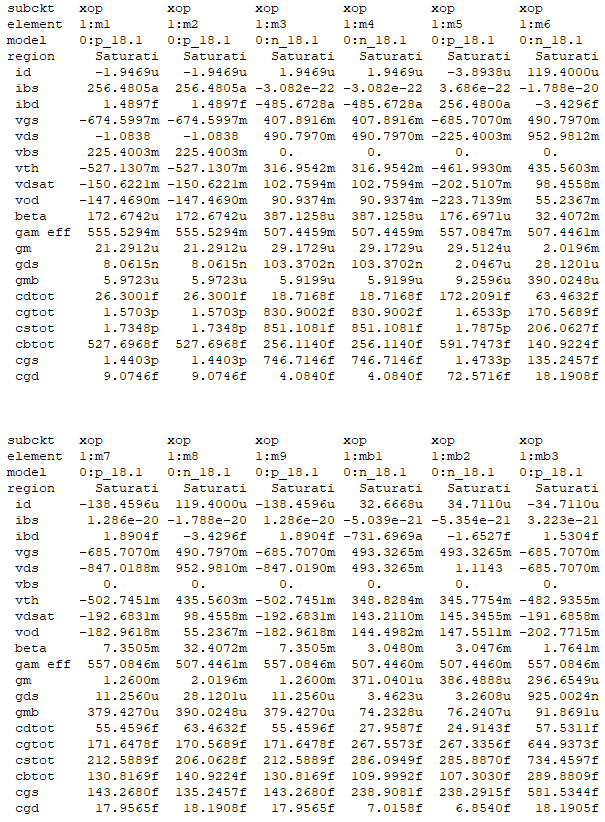
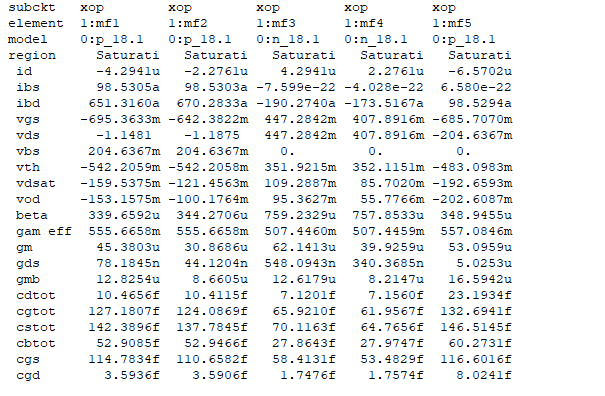


Fig. 1(b) node voltage & branch current



List.1-1 small signal parameters of each devices



List.1-2 small signal parameters of each devices

2. Spice code

.param vdd=1.8V \*Yourpositive supply voltage

.param vss=0V \*Your negative supply voltage

.param vocm=0.9V \*Your output common mode voltage(for CMFB)

.SUBCKT op vinp vinn vdd vss vop von vocm

\*\*\*first stage\*\*\*

M1 D13 vinp S51 vdd P\_18 w=25u l=10u m=1

M2 D24 vinn S51 vdd p\_18 w=25u l=10u m=1

M3 D13 vcmc vss vss N\_18 w=13u l=10u m=1

M4 D24 vcmc vss vss N\_18 w=13u l=10u m=1

M5 S51 vb3 vdd vdd p\_18 w=25u l=10u m=1

\*\*\*second stage\*\*\*

M6 von D24 vss vss N\_18 w=50u l=0.5u m=1

M7 von vb3 vdd vdd P\_18 w=50u l=0.5u m=1

M8 vop D13 vss vss N\_18 w=50u l=0.5u m=1

M9 vop vb3 vdd vdd P\_18 w=50u l=0.5u m=1

\*\*\*compensation\*\*\*

RZ1 C1 vop 15k

CC1 D13 C1 1p

RZ2 C2 von 15k

CC2 D24 C2 1p

\*\*\*biasing\*\*\*

MB1 vb1 vb1 vss vss N\_18 w=20u l=2u m=1

MB2 vb3 vb1 vss vss N\_18 w=20u l=2u m=1

MB3 vb3 vb3 vdd vdd P\_18 w=50u l=2u m=1

Rb vdd vb1 40k

\*\*\*CMFB\*\*\*

MF1 DF13 vocm SF51 vdd P\_18 w=10u l=2u m=1

MF2 vcmc RCM SF51 vdd P\_18 w=10u l=2u m=1

MF3 DF13 DF13 vss vss N\_18 w=5u l=2u m=1

MF4 vcmc vcmc vss vss N\_18 w=5u l=2u m=1

MF5 SF51 vb3 vdd vdd P\_18 w=10u l=2u m=1

RCM1 vop RCM 50k

RCM2 von RCM 50k

.ENDS

3. Simulation

3.1 Open-loop differential mode AC response

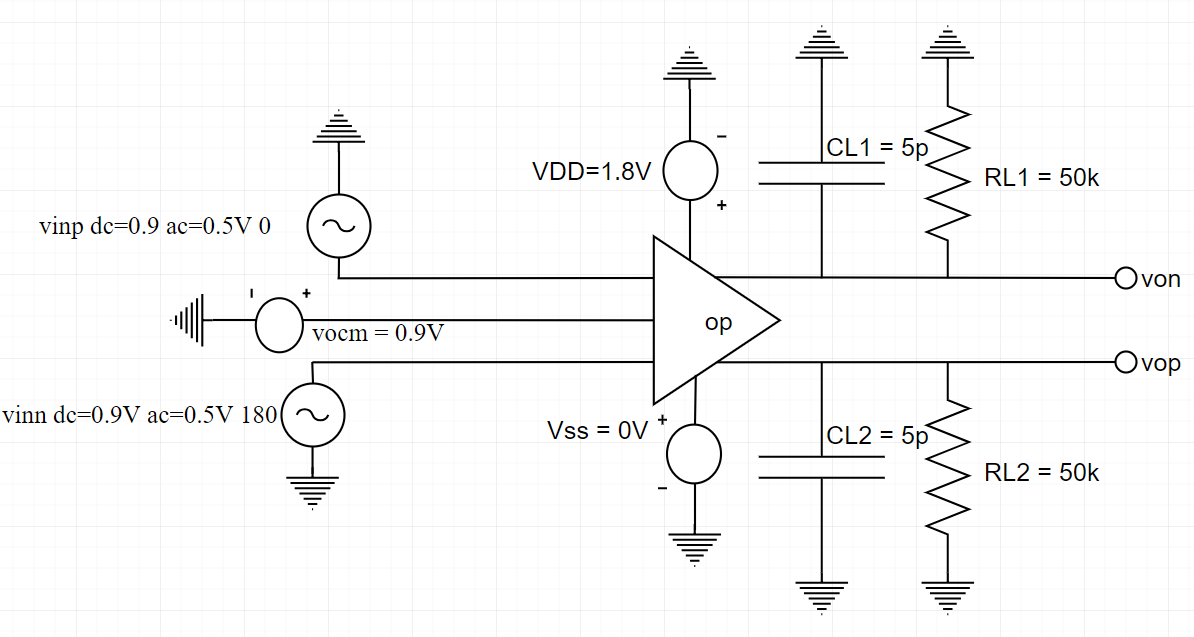


Fig 3-1 (a) test circuit

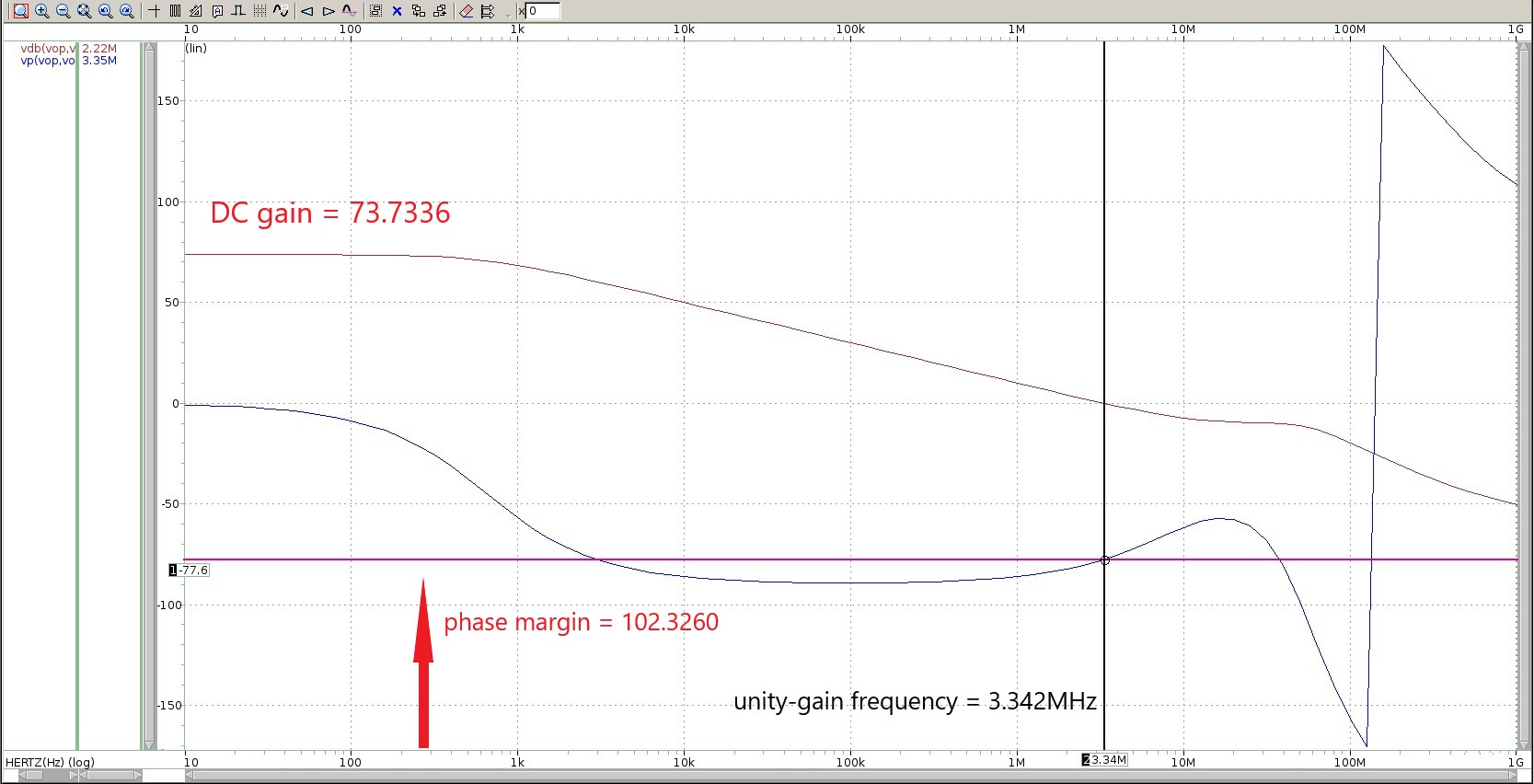


Fig 3-1(b) AC magnitude and phase responses of differential mode gain

縱軸：gain (dB)、phase (degree)

橫軸：frequency (Hz)

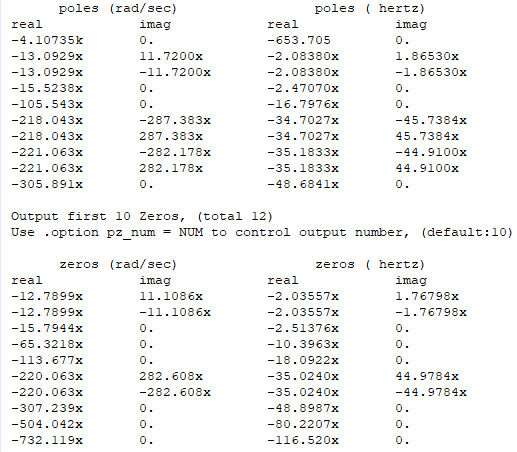


Fig 3-1(c) .pz result

(d) hand calculations：

gain = gm1\*(ro1//ro3)\*gm8\*(r08//ro9//) = 79.94 dB (close to simulation！)

pole1 = 290 Hz

pole2 == 63.95 MHz

zero = = 10.9 MHz

如果把相近的pole跟zero消去，那simulation的結過應為：pole1 = 653.705 Hz、pole2 = 48.6841 MHz、zero = 10.3963 MHz，這樣就與手算有些許誤差，推測是忽略寄生電容影響造成！

3.2 Open-loop differential mode DC sweep

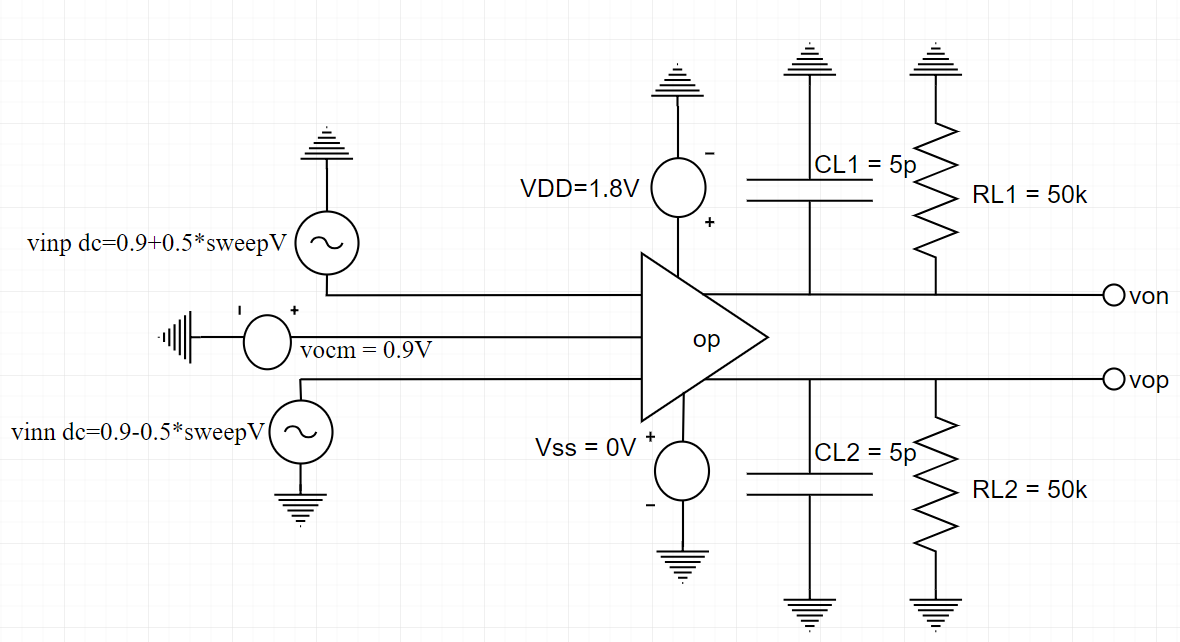


Fig 3-2 (a) test circuit

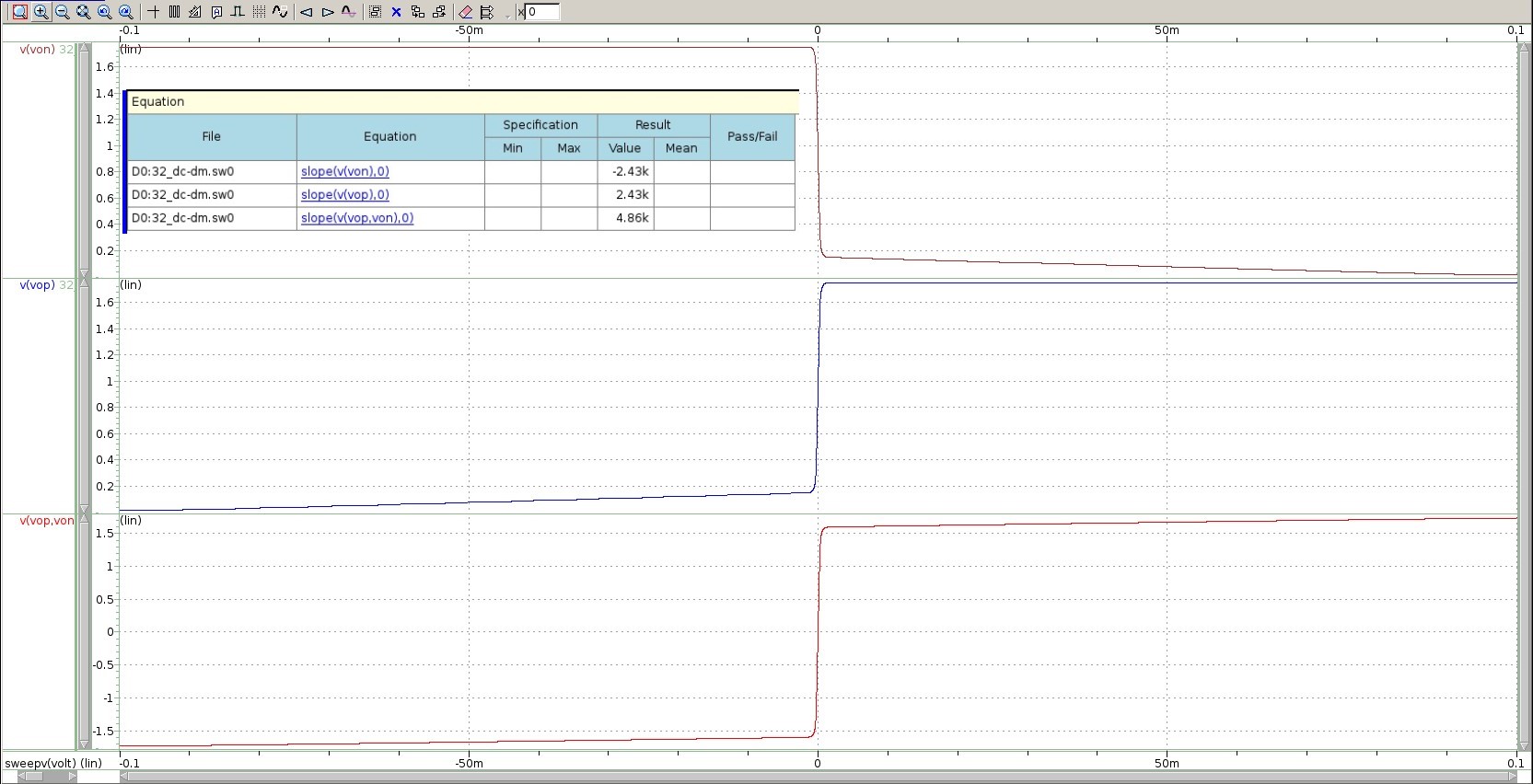


Fig 3-2 (b) single-ended and differential outputs for inputs with differential signals

縱軸：von、vop、vop-von (V)

橫軸：vinn (V)

AC response：gain = 4.8605k (match！)

3.3 Open-loop common mode AC response

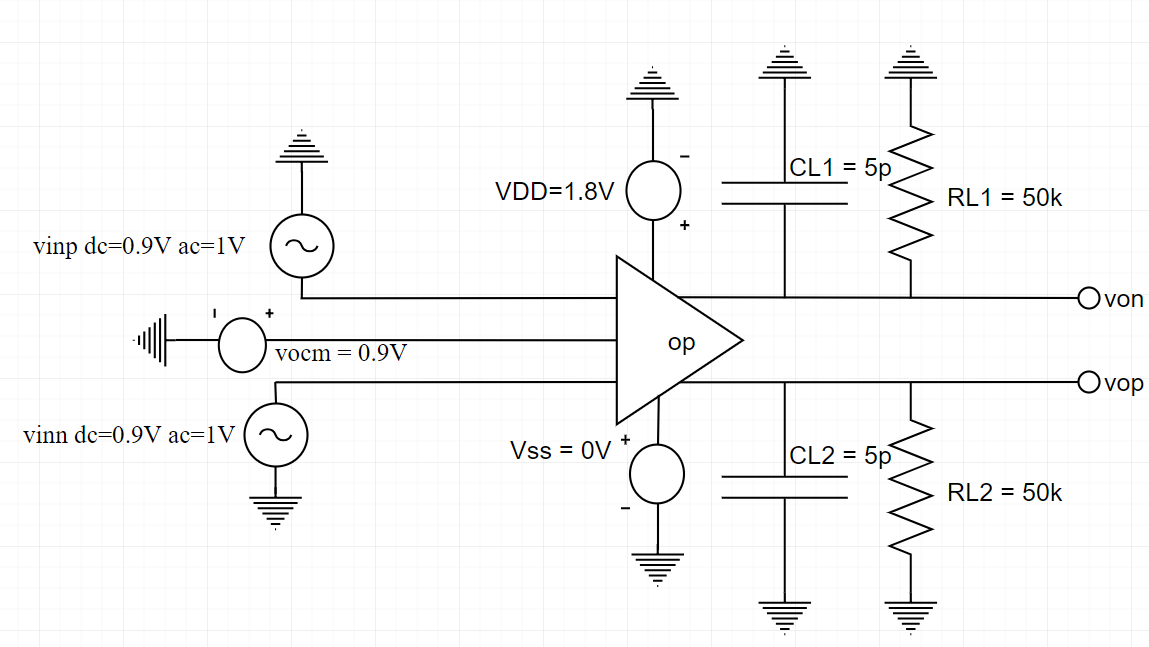


Fig 3-3 (a) test circuit

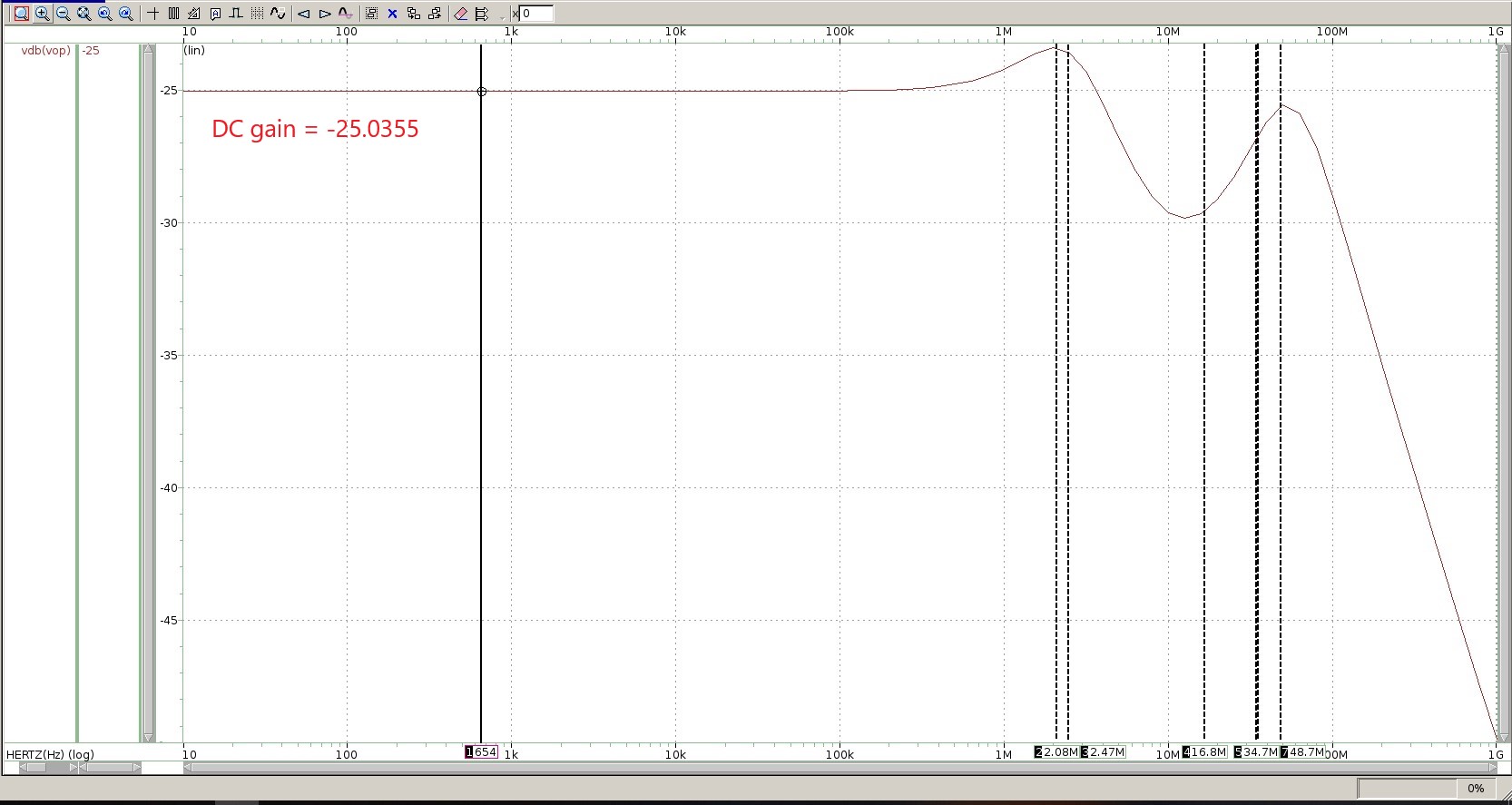


Fig 3-3 (b-1) magnitude response of common mode gain (poles)

縱軸：gain (dB)

橫軸：frequency (Hz)

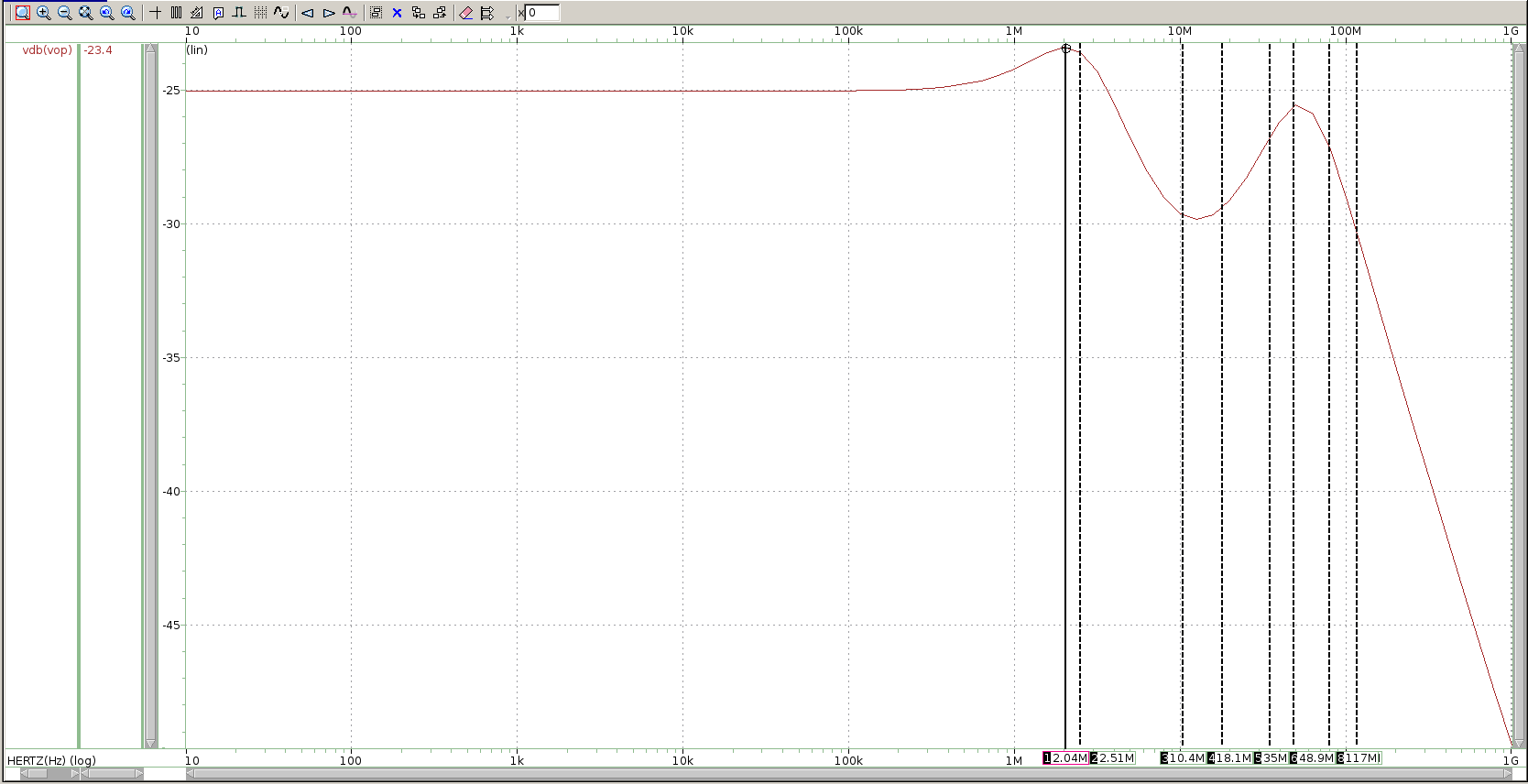


Fig 3-3 (b-2) magnitude response of common mode gain (zeros)

縱軸：gain (dB)

橫軸：frequency (Hz)

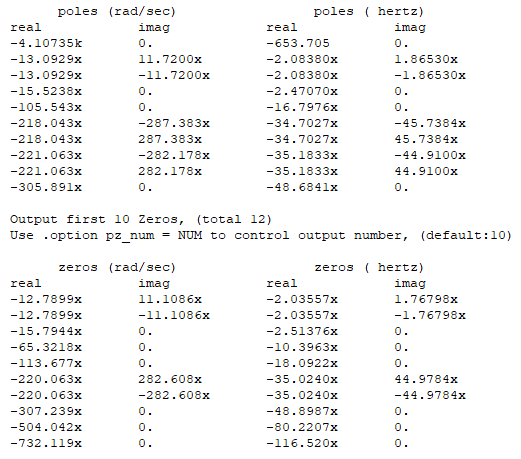


Fig 3-3 (c) .pz result

(d) hand calculations

Common mode gain = = -18.94 dB (可能因估算粗略並忽略許多內阻故有此誤差！)

pole1 = 290 Hz

pole2 == 63.95 MHz

zero = = 10.9 MHz

如果把相近的pole跟zero消去，那simulation的結過應為：pole1 = 653.705 Hz、pole2 = 48.6841 MHz、zero = 10.3963 MHz，這樣就與手算有些許誤差，推測是忽略寄生電容影響造成！

3.4 Open-loop common mode DC sweep

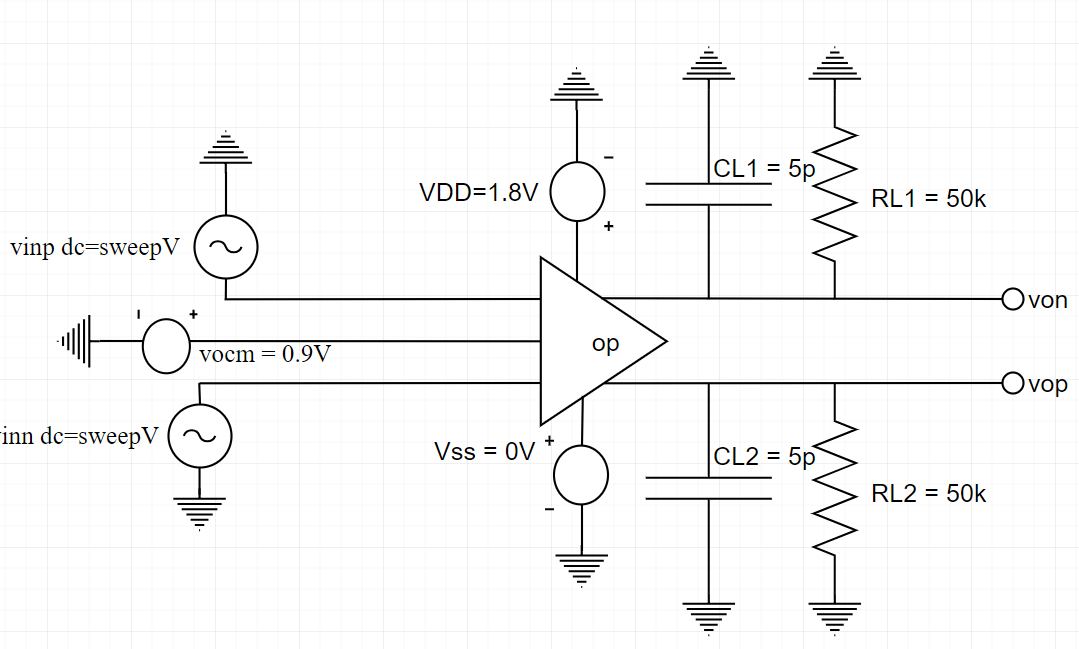


Fig 3-4 (a) test circuit

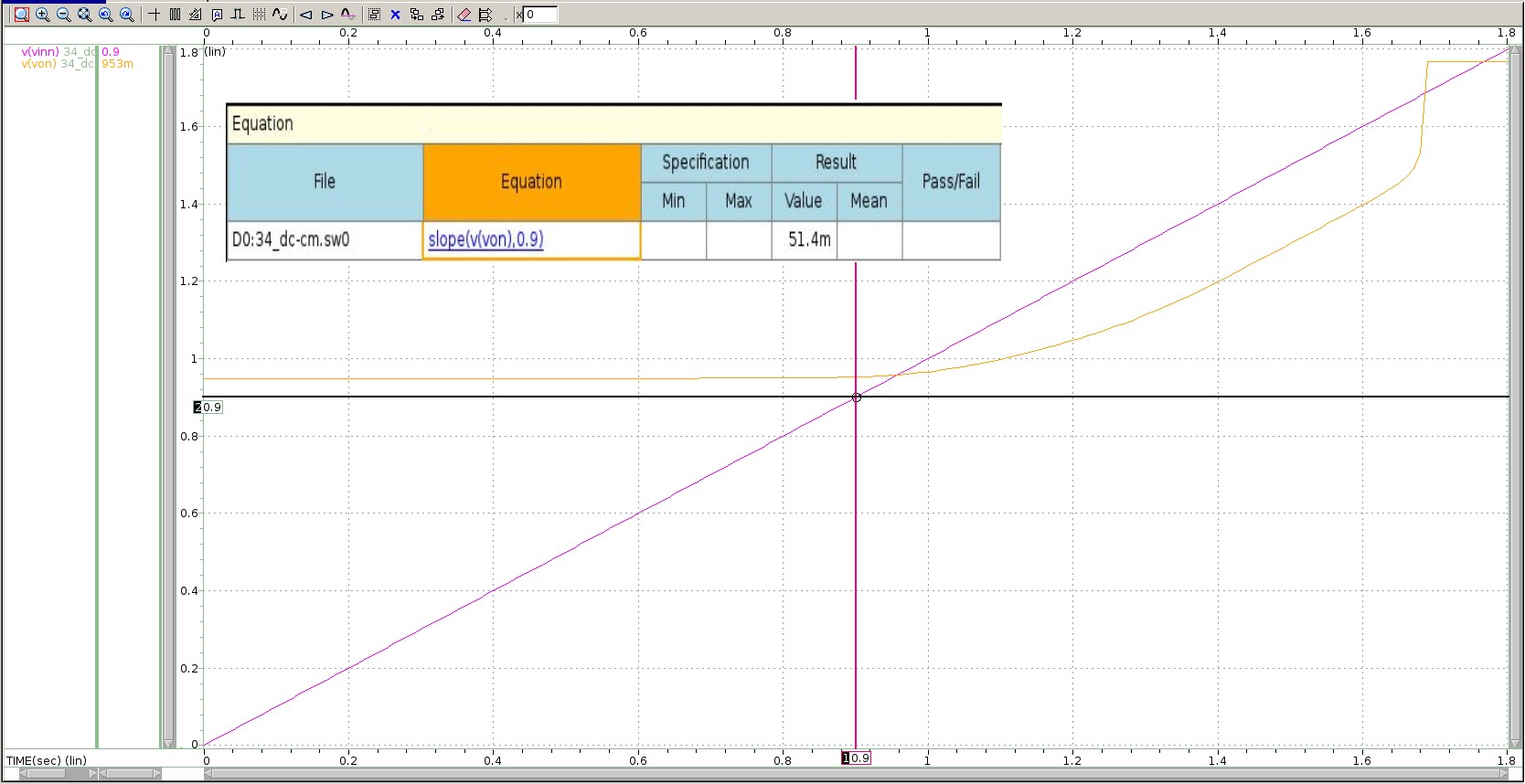


Fig 3-4 (b) outputs for inputs with common mode signals

縱軸：von、vinn (V)

橫軸：vinn (V)

AC response：gain = -25.0355 dB (very close to DC = 0.9V：-25.7807 dB)

3.5 Open-loop power supply+ AC response

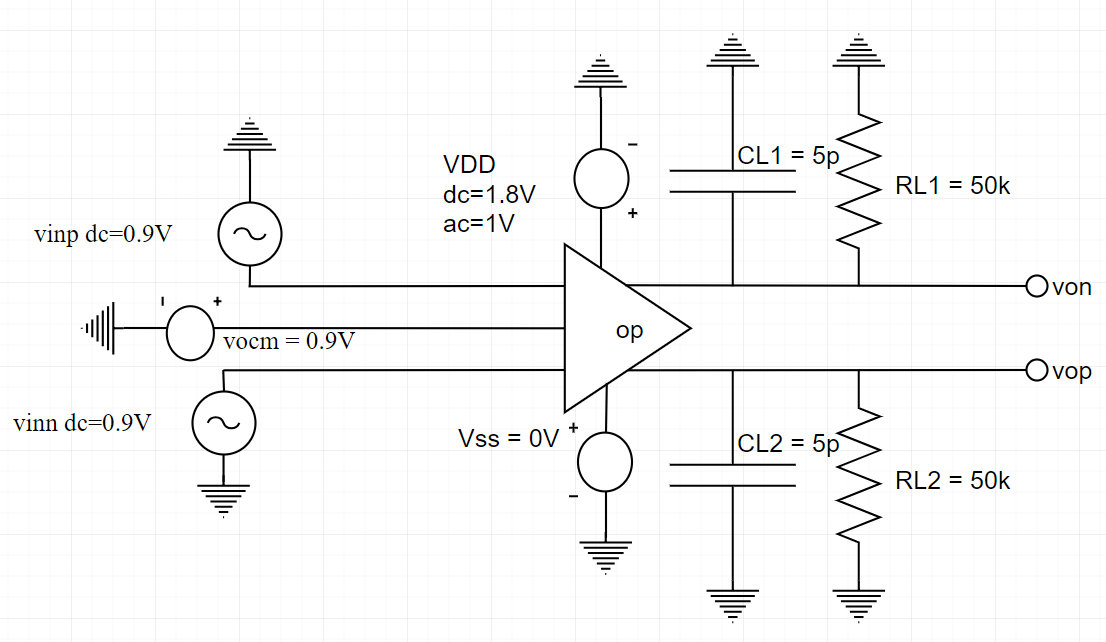


Fig 3-5 (a) test circuit

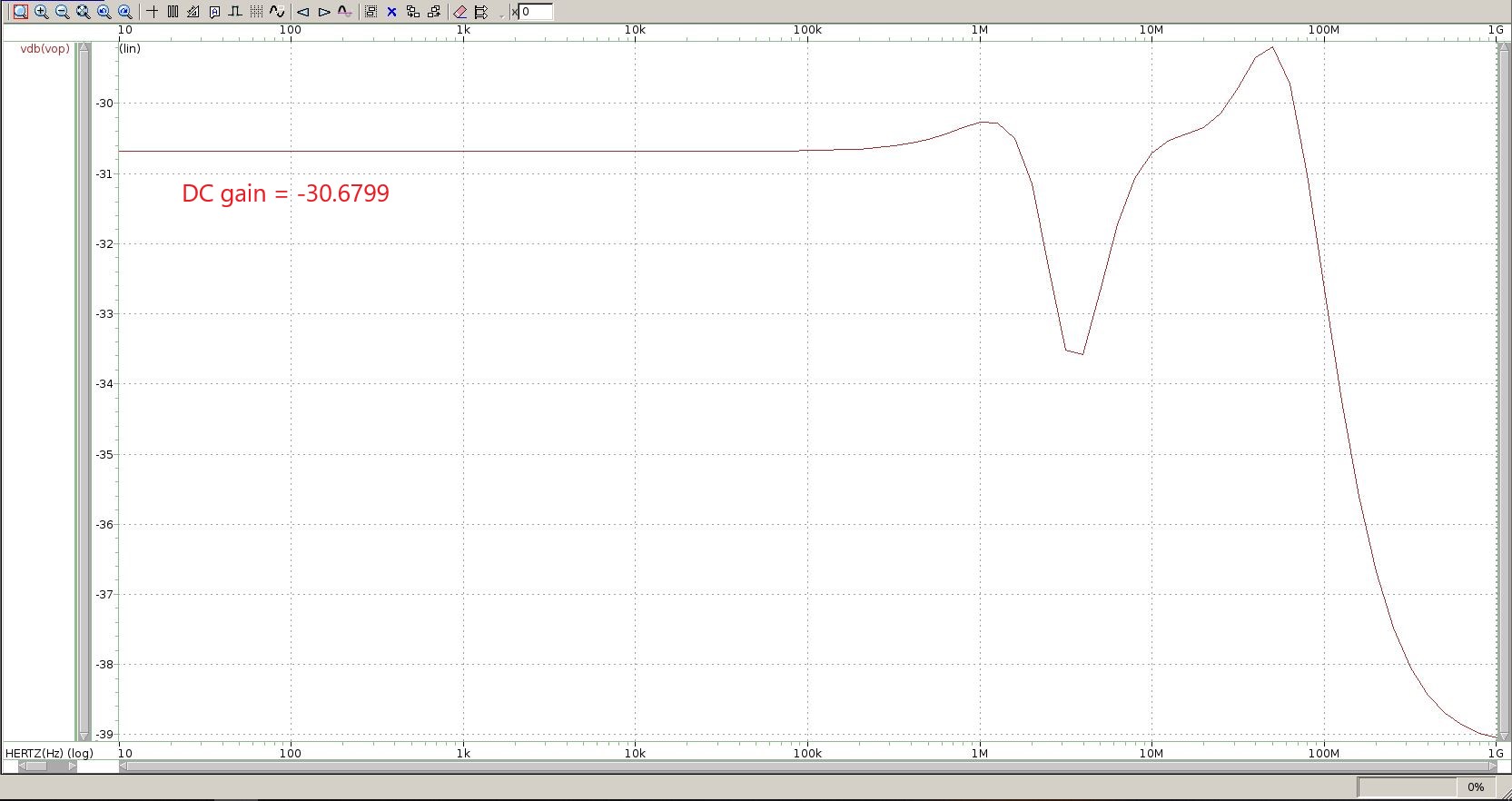


Fig 3-5 (b) magnitude response of power supply+gain

縱軸：gain (dB)

橫軸：frequency (Hz)

3.6 Open-loop power supply-AC response

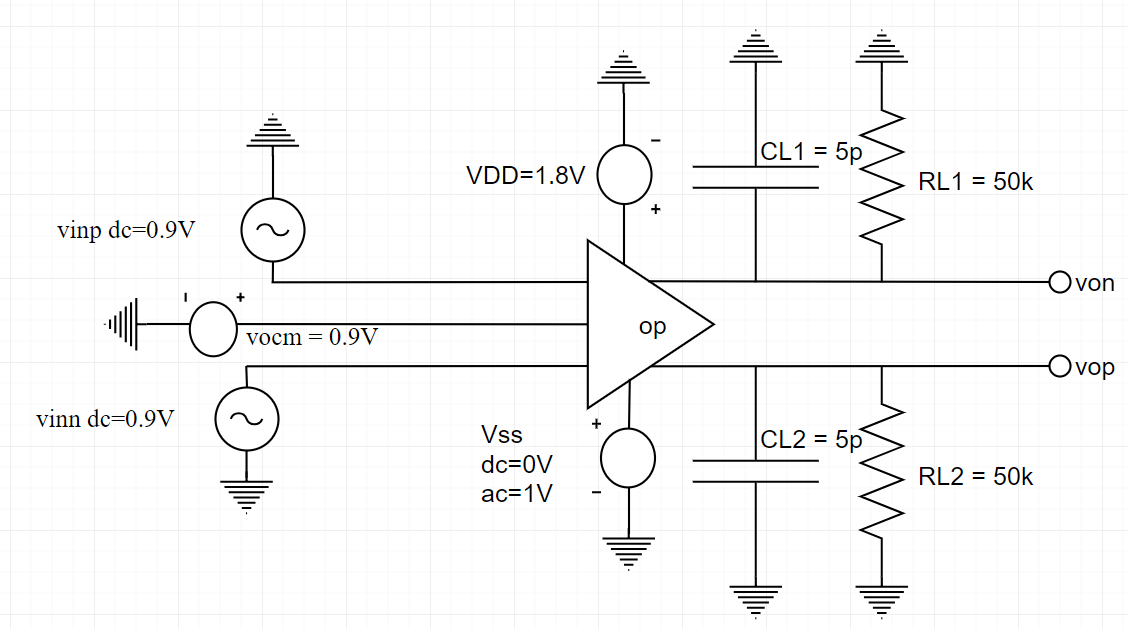


Fig 3-6 (a) test circuit

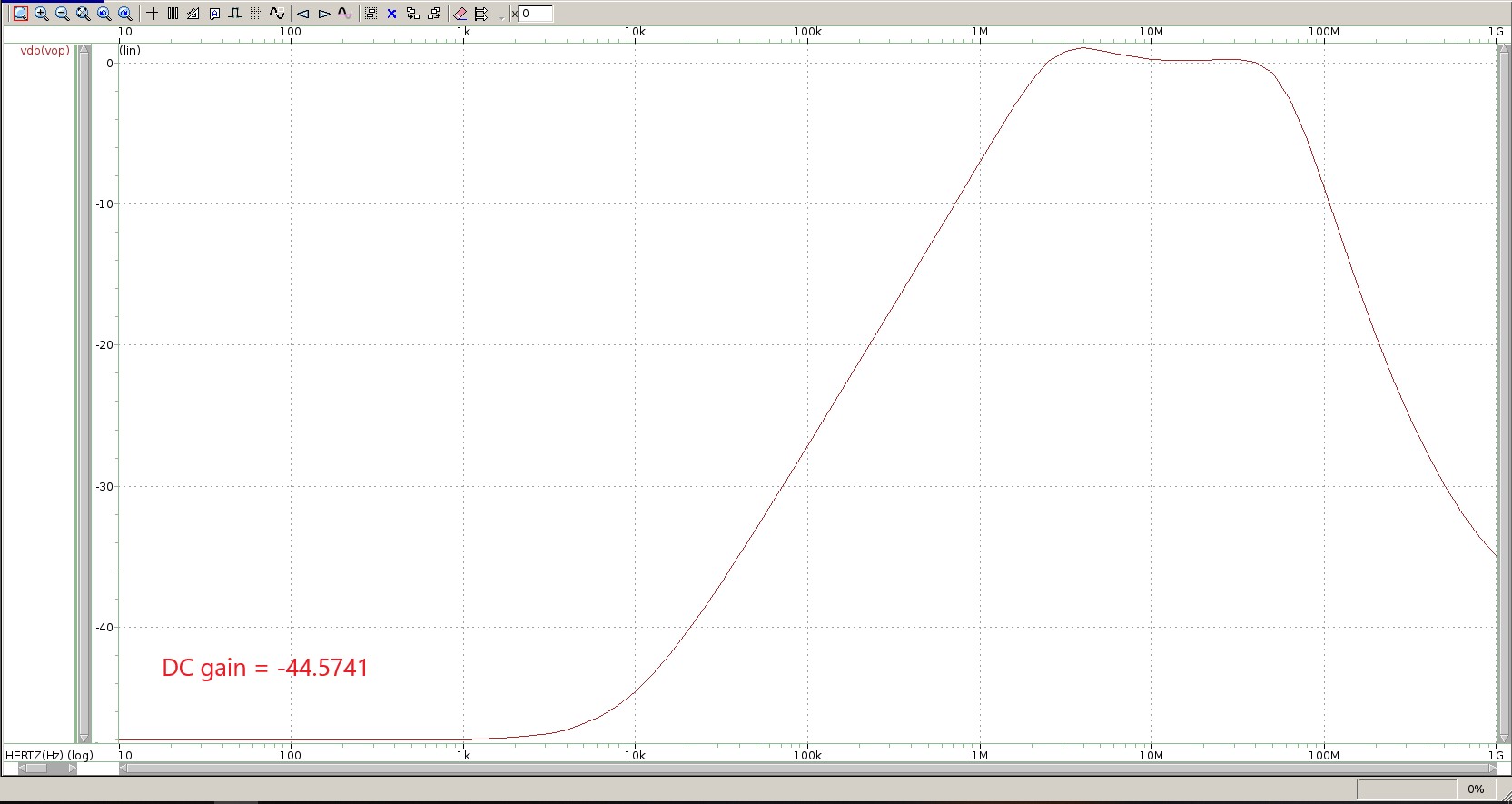


Fig 3-6 (b) magnitude response of power supply-gain

縱軸：gain (dB)

橫軸：frequency (Hz)

3.7 Closed-loop differential mode AC response

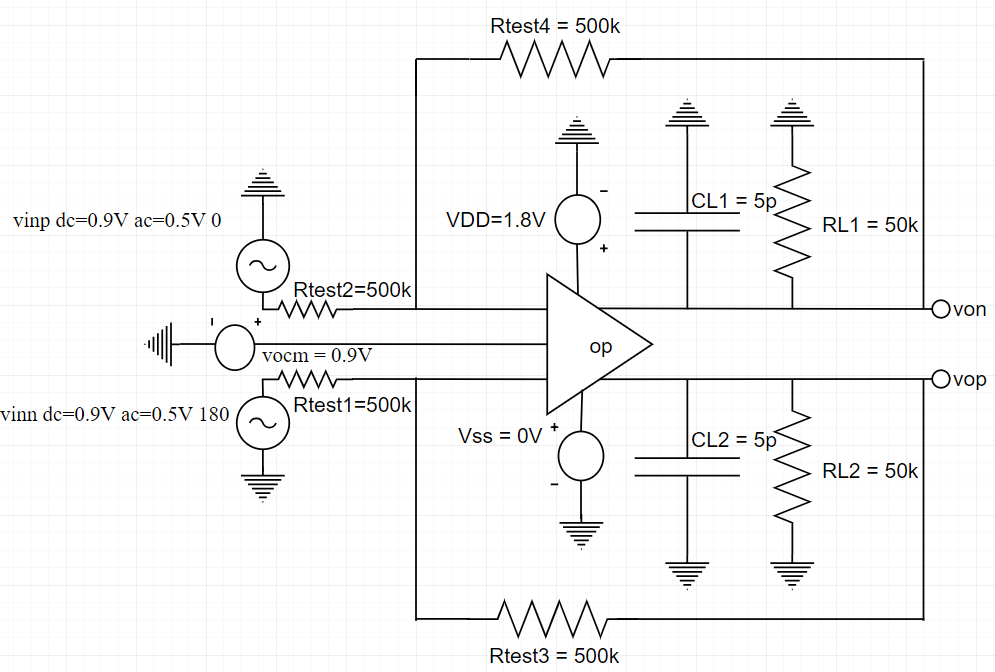


Fig 3-7 (a) test circuit

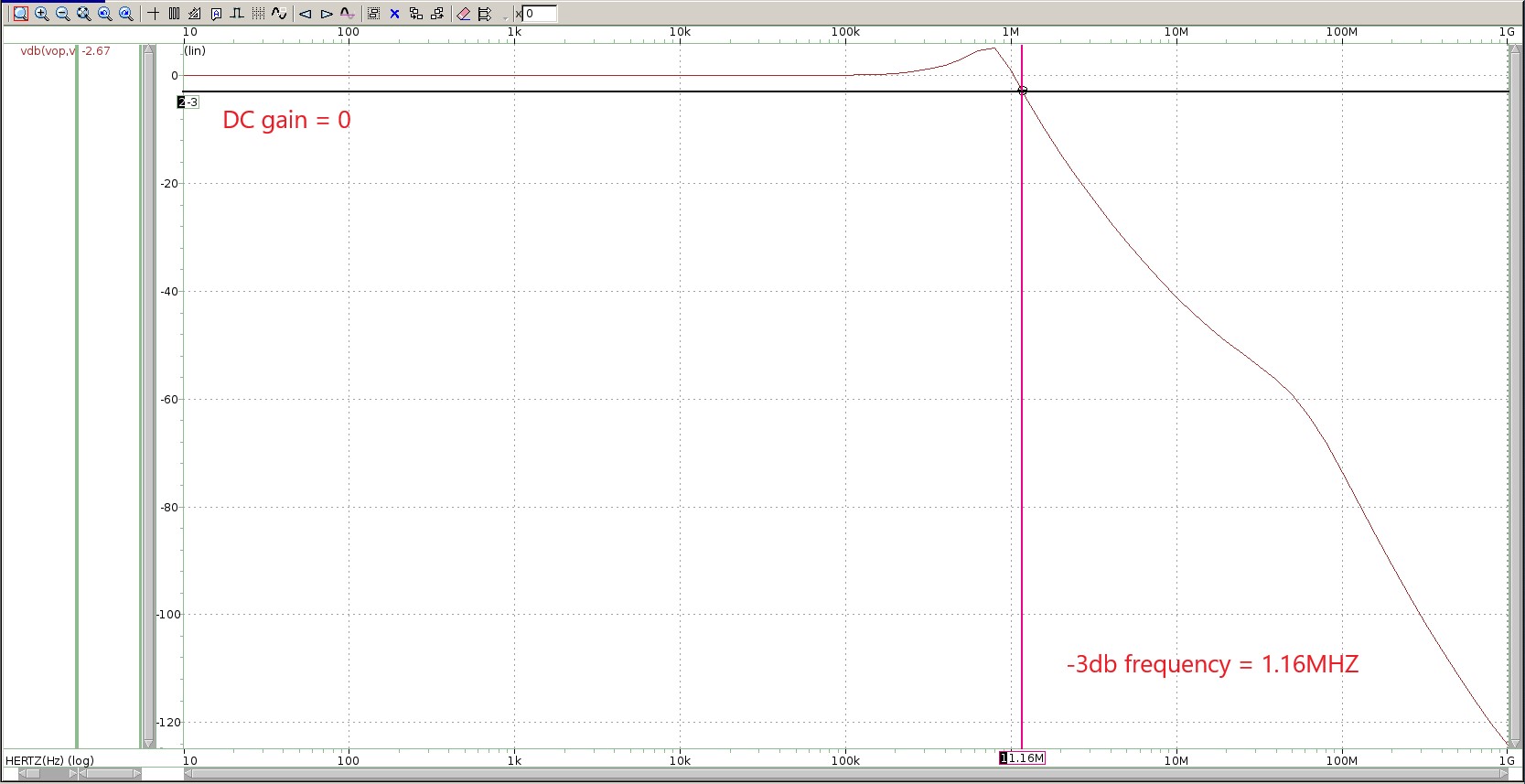


Fig 3-7 (b) AC magnitude and phase responses of differential mode gain

縱軸：gain (dB)

橫軸：frequency (Hz)

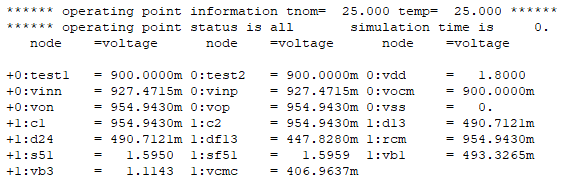


Fig 3-7 (c) input and output node voltages

input node：test1, test2 (voltage both = 0.9V reasonable！)

output node：vin, vop (both 954.943mV reasonable！)

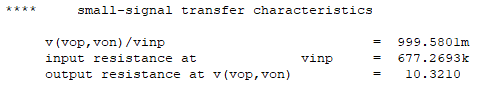


Fig 3-7 (d) .tf result

(e)

Closed loop gain = , k is feedback gain (=0.5), A is open loop gain.

* Closed loop gain = 999.589m (very close to simulation！)

3.8 Closed-loop differential mode DC sweep

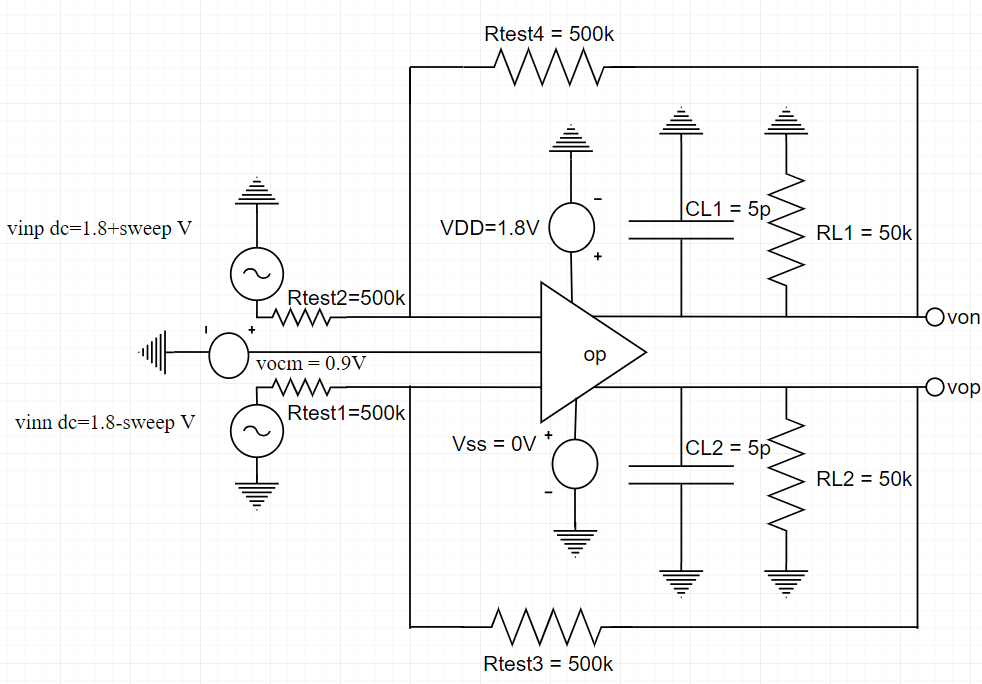


Fig 3-8 (a) test circuit

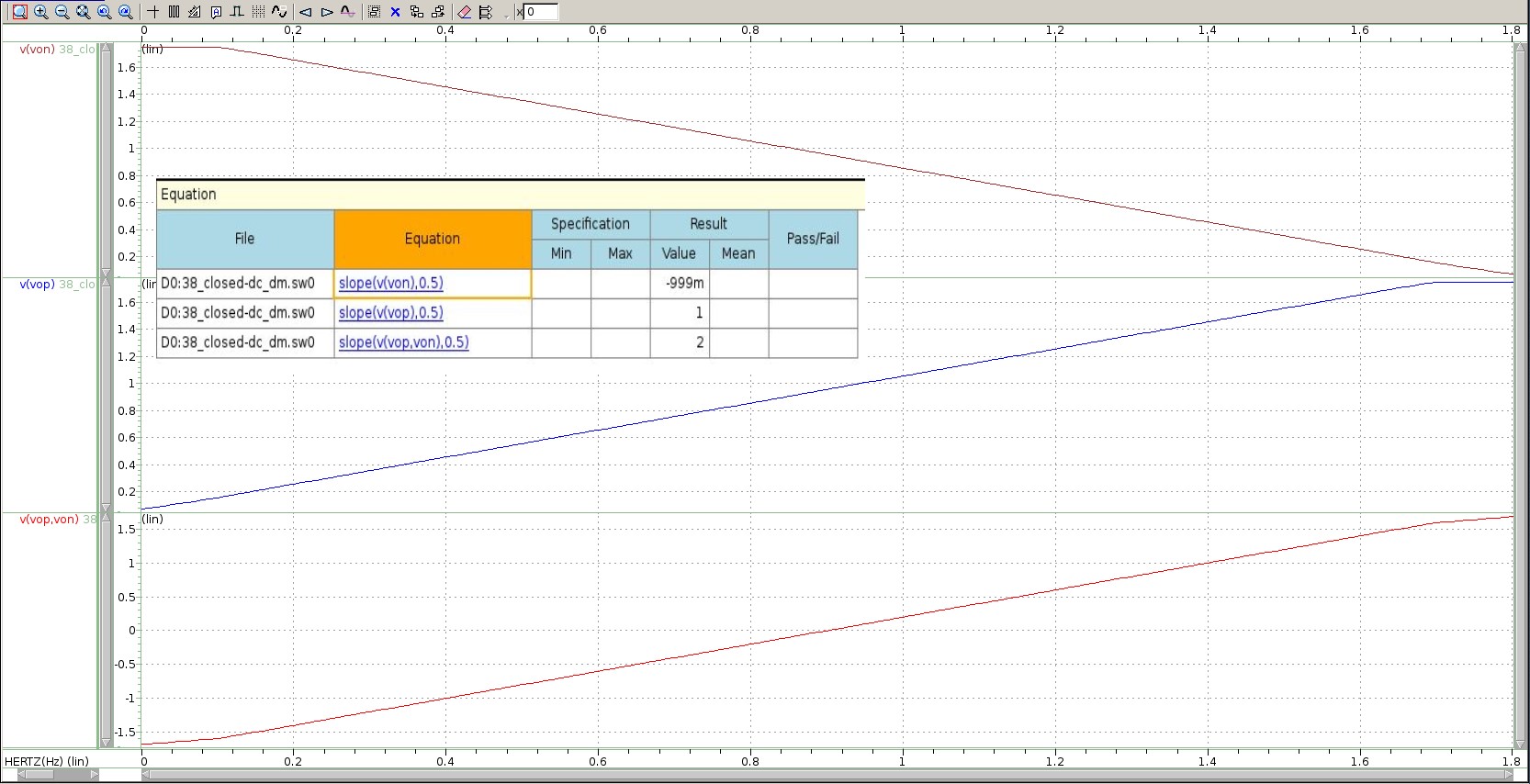


Fig 3-8 (b) single-ended and differential outputs for inputs with differential signals

縱軸：von、vop、vop-von (V)

橫軸：vinn (V)

AC gain (overshoot)：5.0752dB (close to DC gain：6.0205dB)

3.9 Closed-loop step+response

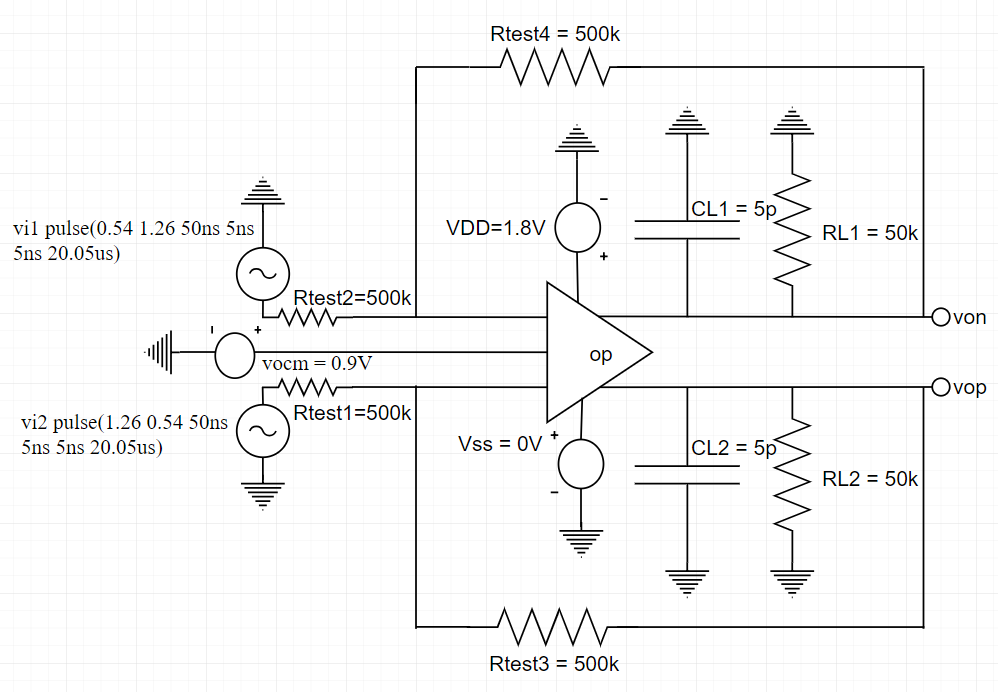


Fig 3-9 (a) test circuit

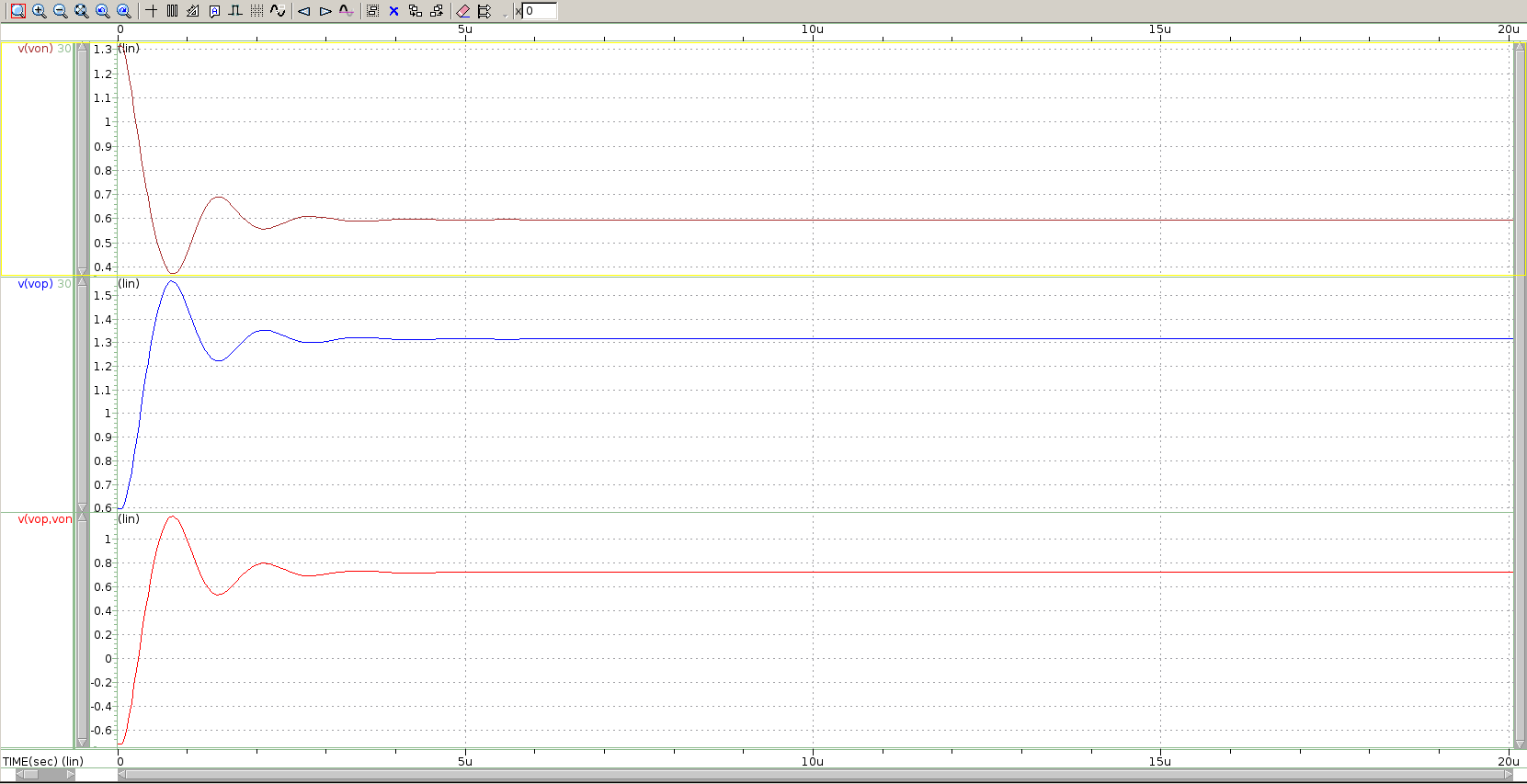


Fig 3-9 (b) single-ended and differential outputs for 1.44V differential step inputs

縱軸：von、vop、vop-von (V)

橫軸：time (sec)

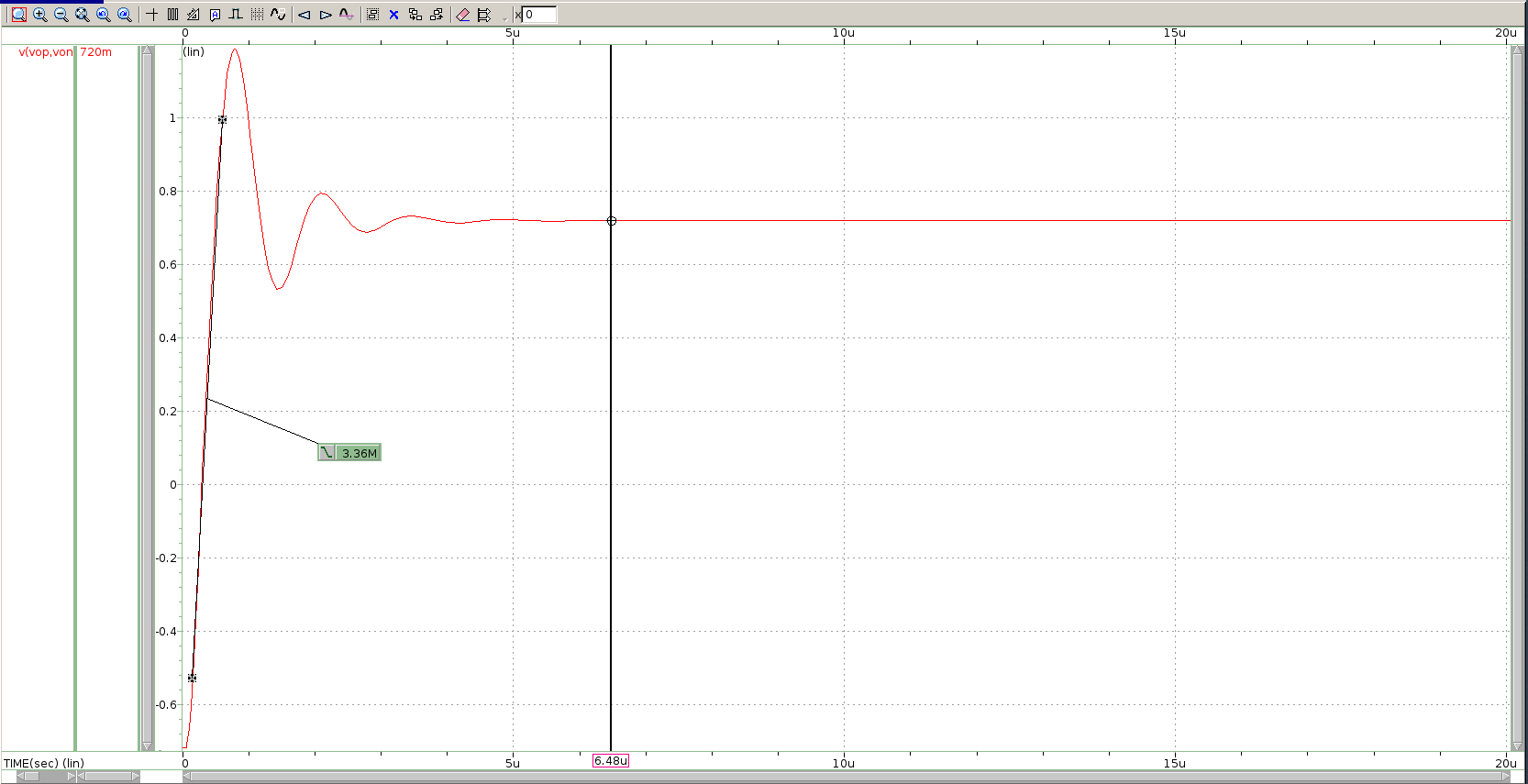


Fig 3-9 (c) slew rate and settling time (6.48u)

縱軸：von、vop、vop-von (V)

橫軸：time (sec)

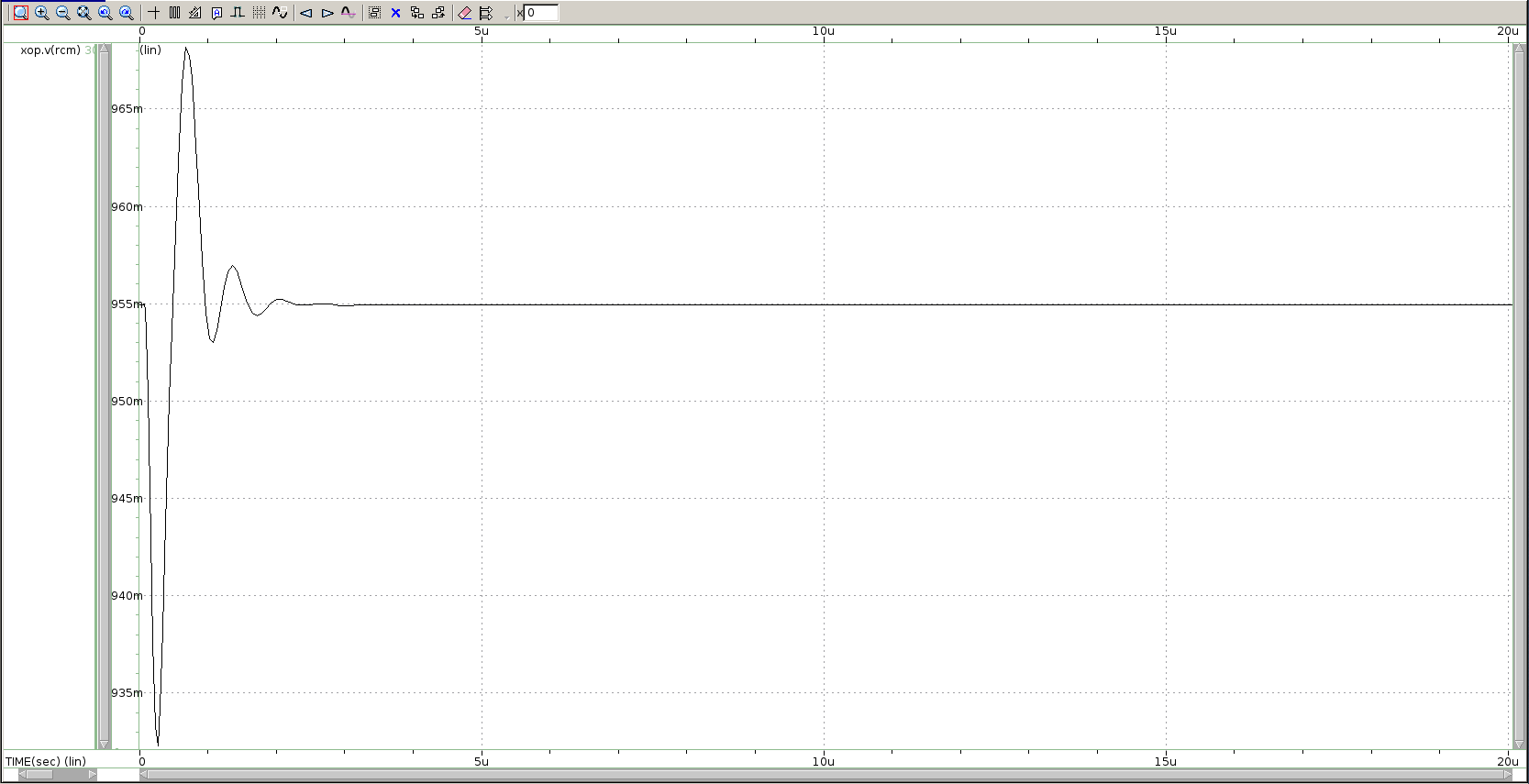


Fig 3-9 (d) common mode sensing node waveform

縱軸：common mode output (V)

橫軸：time (sec)

(e)

By assistant of vocm as reference voltage, CMFB tend to make the common mode output voltage be the same as vocm. When common mode output voltage increase causing the current of MF2、MF4 will decrease, so voltage of vcmc will decrease and drain voltage of M4 also decrease leading the common mode output voltage decrease. When common mode output voltage decrease causing the current of MF2、MF4 will increase, so voltage of vcmc will increase and drain voltage of M4 also increase leading the common mode output voltage will increase.

3.10 Closed-loop step-response

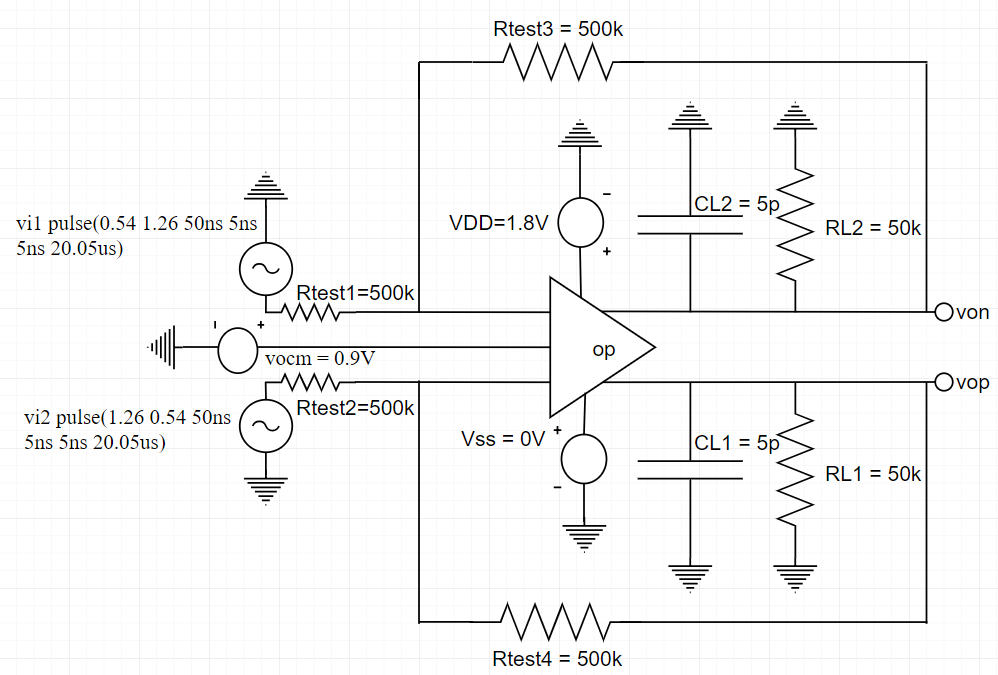


Fig 3-10 (a) test circuit

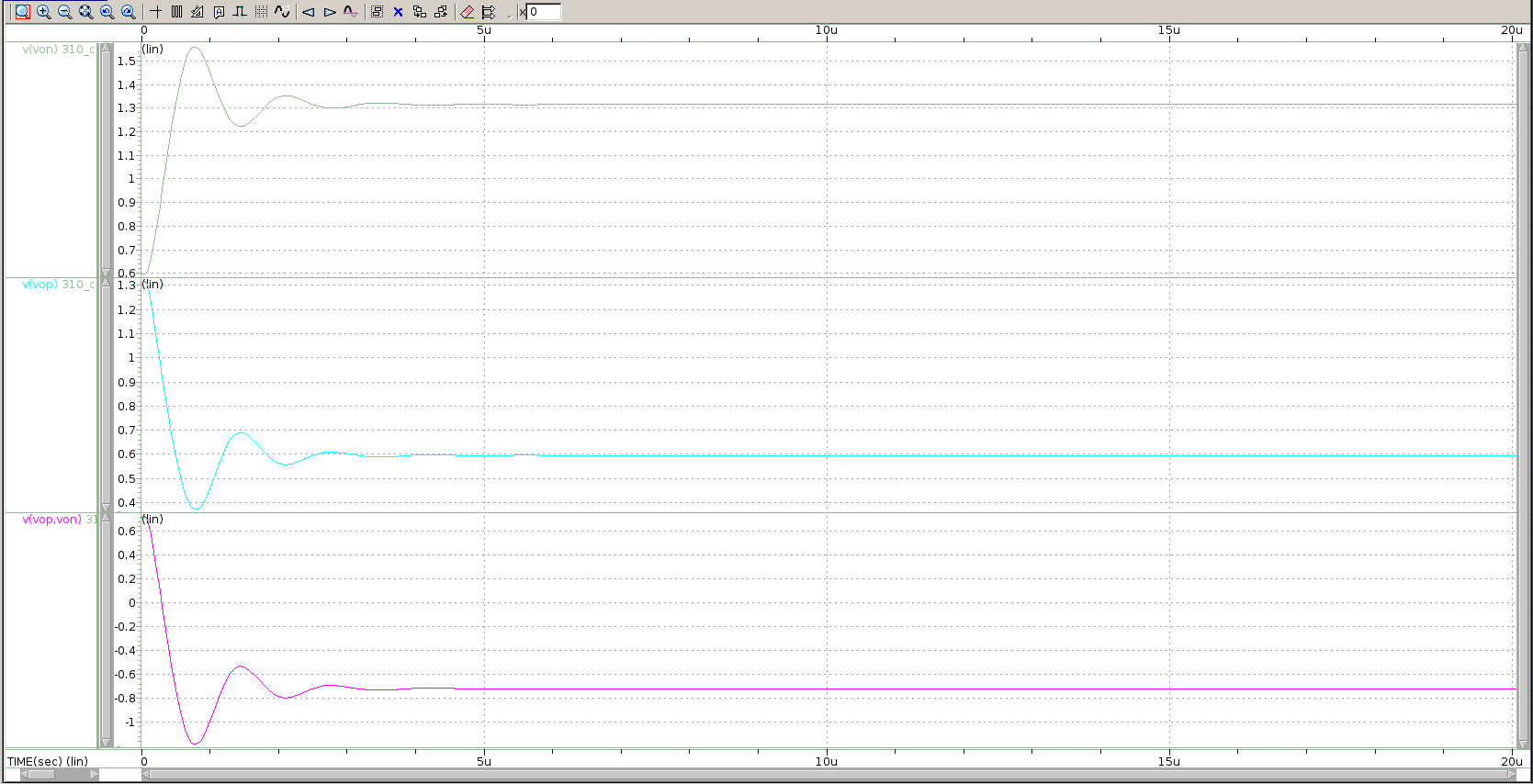


Fig 3-10 (b) single-ended and differential outputs for -1.44V differential step inputs

縱軸：von、vop、vop-von (V)

橫軸：time (sec)

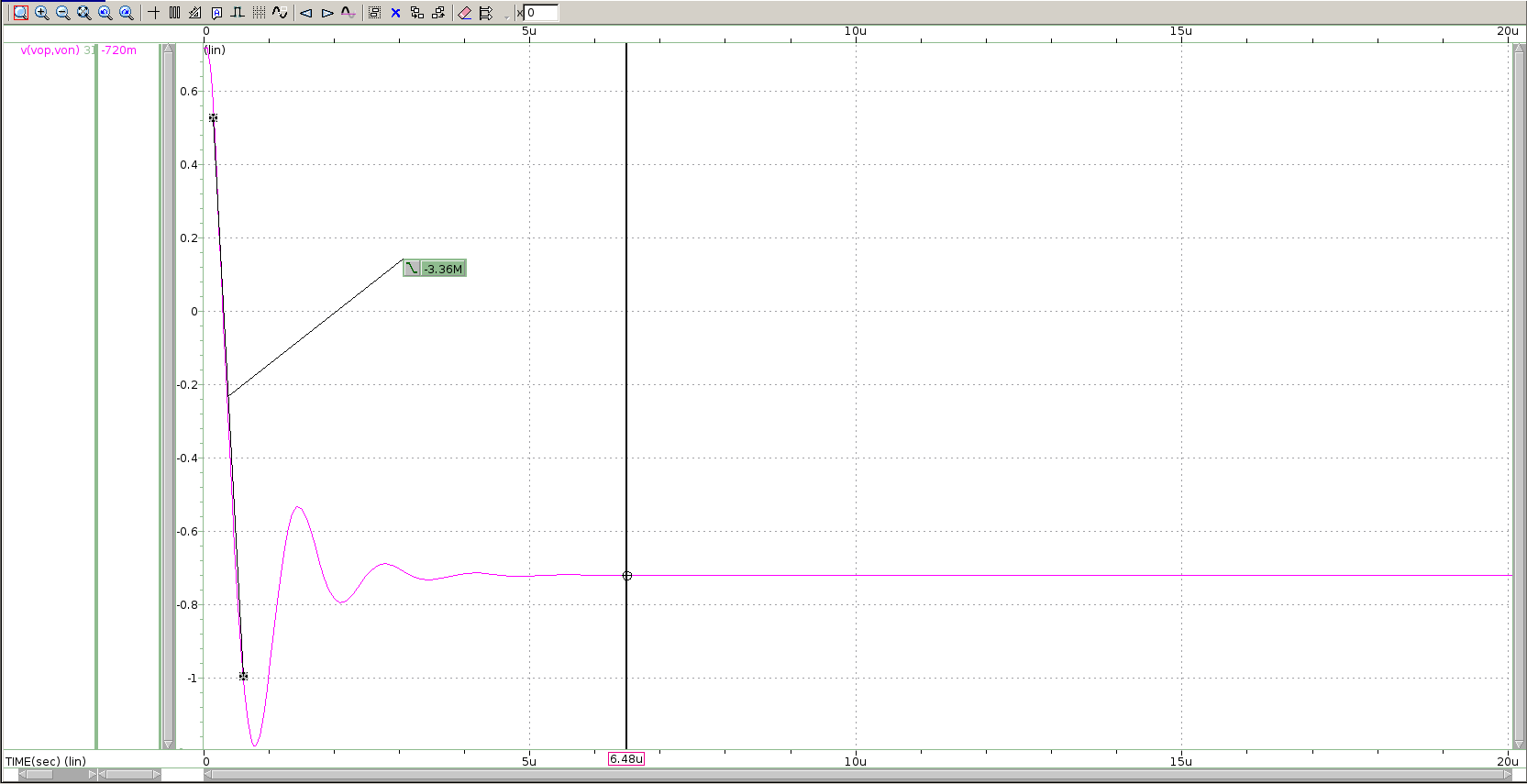


Fig 3-10 (c) slew rate and settling time

縱軸：von、vop、vop-von (V)

橫軸：time (sec)

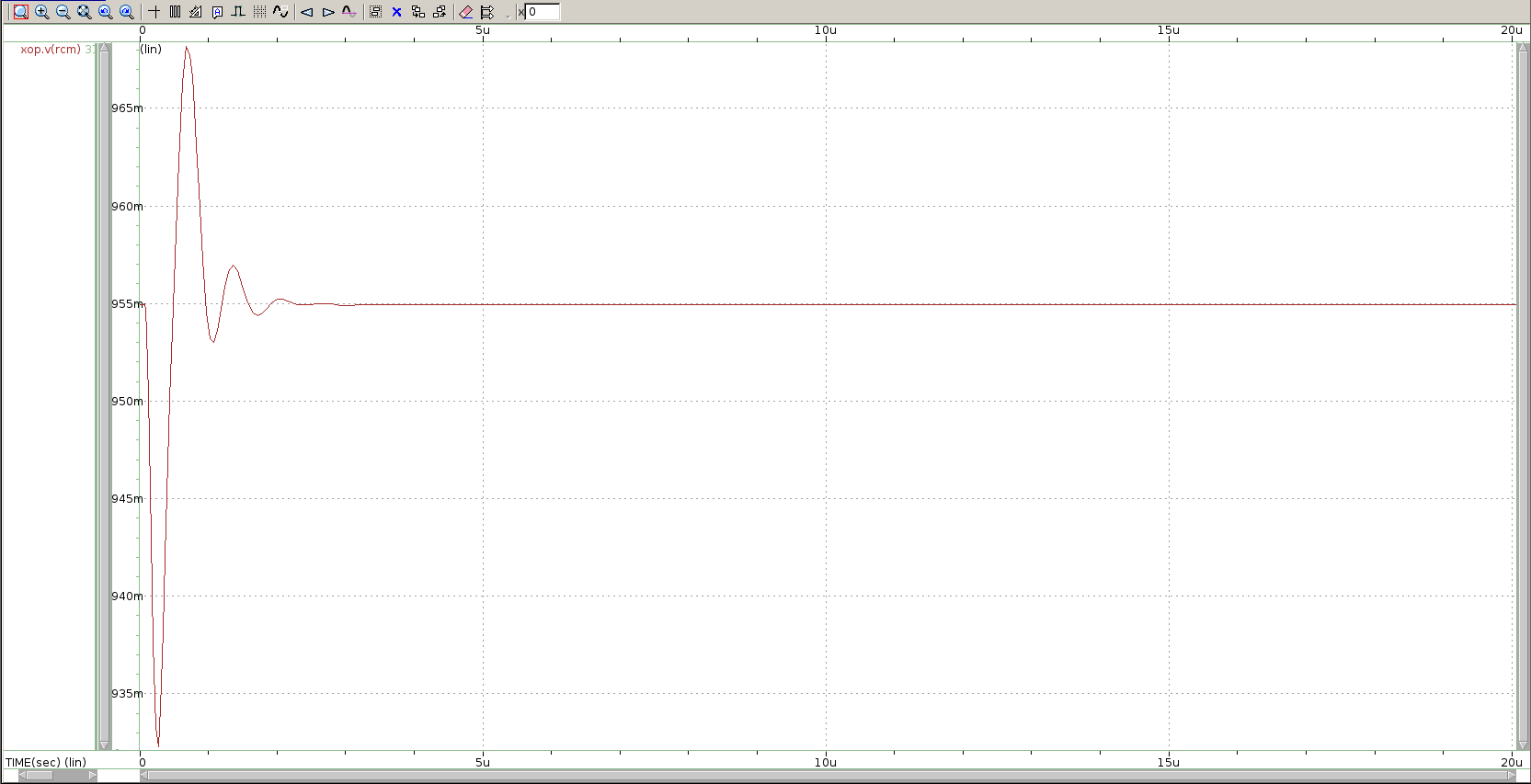


Fig 3-9 (d) plot the common mode sensing node waveform

縱軸：common mode output (V)

橫軸：time (sec)

4. Performance Table

|  |  |  |
| --- | --- | --- |
| Design Items | Specifications | My Work |
| Technology | CIC pseudo 0.18um technology | |
| Supply Voltage | **1.8V**, as small as possible | 1.8V |
| Vicm, Vocm | **0.9V / 0.9V** | 0.9V / 0.9V |
| Supply Current (Total) | **< 4mA**, as small as possible | -354.761u |
| Loading | 5pF / 50KΩ (for each output) | 5pF / 50KΩ |
| Compensation R, C | Open for design | 15KΩ / 1pF |
| Open-loop simulation | | |
| DC gain | **> 72dB**, as large a possible | 73.7336 dB |
| Unity-GBW | **> 1MHz**, as large as possible | 3.3420 MHz |
| P.M. | **> 45°** | 102.326 |
| C.M.R.R. @10KHz | > 80dB | 98.7691 dB |
| P.S.R.R.+ @10KHz | > 80dB | 104.4135 dB |
| P.S.R.R.- @10KHz | > 80dB | 118.3077 dB |
| Closed-loop simulation | | |
| Differential swing of 1.44V (step signal) | | |
| S.R.+ (10% ~ 90%) | > 1 V/us | 3.36V/us |
| S.R.- (10% ~ 90%) | > 1 V/us | -3.36V/us |
| Settling+ (to 0.1%) | < 10 us | 6.4834u |
| Settling- (to 0.1%) | < 10 us | 6.4834u |
| FoM | | |
| Small signal | GBW (MHz) \* CL (pF) / Power( mW ) | 26.17 |
| Large signal + | SR+(V/us) \* CL (pF) / Power( mW ) | 26.31 |
| Large signal - | SR-(V/us) \* CL (pF) / Power( mW ) | -26.31 |

5. Design Concerns

首先把bias circuit拔掉改接電壓源來測試我的gain以及GBW有沒有到要求以及MOS有沒有在saturation。成功後就開始設計bias circuit，讓它可以提供跟電壓源一樣的電壓。同時為了讓slew rate在要求下，所以除了RCM以外都盡量追求小的阻值(MOS size小、R小、C小)。而為了使CMFB可以正常運作，所以兩個RCM取一樣的大小並讓它遠大於output resistance。

6. Discussions

這次的Final讓我了解到類比電路設計需要非常紮實的電子電路學基礎以及上網找資料的能力。不只這次project，這學期的作業有許多資料都必須上網查或是回去溫習之前學過的課程，訓練了我們解決問題的能力。跟之前作業不同的是這次Final的電路比較複雜，因此上手比較需要時間理解，當徹底了解電路的結構以及功用後在調size上就不會很有障礙，相信之後再遇到類似的問題或是更複雜的電路便能像這樣先解構它了解原理後再開始設計會節省許多時間。